CLAIM(S)

What is claimed is:

1. An apparatus for supplying current to a semiconductor device during a test of the semiconductor device by an integrated circuit tester accessing input/output (I/O) terminals of the semiconductor device via interface means providing signal paths between the I/O terminals and the integrated circuit tester, wherein the semiconductor device includes a power input terminal for receiving supply current via a power conductor provided by the interface means, and wherein the semiconductor device temporarily increases its demand for supply current following each of a set of edges of a clock signal applied as input to the semiconductor device, the apparatus comprising:

first means for supplying a first current to the power input terminal during the test;

second means for supplying a current pulse to the power input terminal following each of the edges of the clock signal supplementing the first current, wherein a magnitude of the current pulse is a function of magnitudes represented by a prediction signal and an adaption signal; and

third means for adjusting the magnitude represented by the adaption signal in response to a voltage appearing at the power input terminal,

wherein the magnitude represented by the prediction signal is set proportional to a predicted amount by which the semiconductor device will increase its demand for current at its power input terminal following a next one of the clock signal edges.

2. The apparatus in accordance with claim 1, wherein the integrated circuit tester generates the prediction signal.

3. The apparatus in accordance with claim 1 wherein the magnitude of the current pulse is proportional to a product of the magnitudes represented by the prediction signal and the adaption signal.

4. The apparatus in accordance with claim 1 wherein the magnitude represented by the adaption signal is a function of a time varying portion of the voltage appearing at the power input terminal integrated over time.

5. The apparatus in accordance with claim 4 wherein the third means comprises:

means for filtering the voltage appearing at the power input terminal to produce a filtered voltage of magnitude proportional to a variation in magnitude of the voltage appearing at the power input terminal; and

means for integrating the filtered voltage to produce the adaption signal.

6. The apparatus in accordance with claim 1 wherein the second means comprises:

a digital-to-analog converter for receiving the prediction signal and for generating an analog signal of magnitude proportional to the magnitude represented by the prediction signal;

an amplifier having a gain controlled by the adaption signal; and

means for temporarily applying the analog signal as input to the amplifier following each of the clock signal edges, such that the amplifier produces a current pulse following each of the
clock signal edges wherein the magnitude of the current pulse is a function of the magnitude of the analog signal and the magnitude represented by the adaption signal.

7. The apparatus in accordance with claim 1 wherein the second means comprises:

an amplifier;

means responsive to the prediction signal and the adaption signal for generating an analog signal having a magnitude that is a function of the magnitudes represented by the prediction signal and the adaption signal, and

means for temporarily applying the analog signal as input to the amplifier following each of the clock signal edges, such that the amplifier produces a current pulse following each of the clock signal edges wherein the magnitude of the current pulse is a function of the magnitude of the analog signal.

8. The apparatus in accordance with claim 1 wherein the second means comprises:

an amplifier having a gain controlled by the adaption signal;

a capacitor;

means responsive to the prediction signal for charging a capacitor to a capacitor voltage that is a function of the magnitude represented by the prediction signal prior to each of the clock signal edges; and

means for temporarily connecting the capacitor as input to the amplifier following each of the clock signal edges, such that the amplifier produces a current pulse following each of the clock signal edges wherein the magnitude of the current pulse is a function of the magnitude of the capacitor voltage and the magnitude represented by the adaption signal.

9. The apparatus in accordance with claim 1 wherein the second means comprises:

a power supply producing an output signal of voltage that is a function of the magnitude represented by the prediction signal;

an amplifier powered by the output signal of the power supply and having a gain controlled by the adaption signal; and

means for temporarily applying an analog signal as input to the amplifier following each of the clock signal edges, such that the amplifier produces a current pulse following each of the clock signal edges wherein the magnitude of the current pulse is a function of the voltage of the power supply's output signal and of the magnitude represented by the adaption signal.

10. The apparatus in accordance with claim 1 wherein the interface means comprises a probe board and wherein the second means is mounted on the probe board.

11. The apparatus in accordance with claim 1 wherein the interface means comprises a probe board and wherein the third means is mounted on the probe board.

12. The apparatus in accordance with claim 1 wherein feedback provided by the third means adjusts the magnitude represented by the adaption signal so as to minimize variations in the voltage appearing at the power input terminal.

13. The apparatus in accordance with claim 1,

wherein the integrated circuit tester generates the prediction signal,

wherein the magnitude of the current pulse is proportional to a product of the magnitudes represented by the prediction signal and the adaption signal, and

wherein feedback provided by the third means adjusts the magnitude represented by the adaption signal so as to minimize variations in the voltage appearing at the power input terminal.

14. The apparatus in accordance with claim 13 wherein the interface means comprises a probe board and wherein the second and third means are mounted on the probe board.

15. A method for supplying current to a semiconductor device during a test of the semiconductor device by an integrated circuit tester accessing input/output (I/O) terminals of the semiconductor device via interface means providing signal paths between the I/O terminals and the integrated circuit tester, wherein the semiconductor device includes a power input terminal for receiving supply current via a power conductor provided by the interface means, and wherein the semiconductor device temporarily increases its

demand for supply current following each of a set of edges of a clock signal applied as input to the semiconductor device, the comprising the steps of:

a. supplying a first current to the power input terminal during the test;

b. producing a prediction signal representing a magnitude proportional to a predicted amount by which the semiconductor device will next increase its demand for current at its power input terminal following one of the clock signal edges;

c. producing a adaption signal representing a magnitude determined in response to a voltage appearing at the power input terminal; and

d. supplying a current pulse to the power input terminal following each of the clock signal edges to supplement the first current, wherein a magnitude of the current pulse is a function of magnitudes represented by the prediction signal and the adaption signal.

16. The method accordance with claim 15, wherein the integrated circuit tester carries out step b.

17. The method in accordance with claim 15 wherein the magnitude of the current pulse is proportional to a product of the magnitudes represented by the prediction signal and the adaption signal.

18. The method in accordance with claim 15 wherein the magnitude represented by the adaption signal is a function of a time varying portion of the voltage appearing at the power input terminal integrated over time.

19. The method in accordance with claim 18 wherein step c comprises the substeps of:

c1. filtering the voltage appearing at the power input terminal to produce a filtered voltage of magnitude proportional to a variation in magnitude of the voltage appearing at the power input terminal; and

c2. integrating the filtered voltage to produce the adaption signal.

20. The method in accordance with claim 15 wherein step d comprises the substeps of:

d1. generating in response to the prediction signal an analog signal of magnitude proportional to the magnitude represented by the prediction signal;

d2. temporarily applying the analog signal as input to an amplifier following each of the clock signal edges, such that the amplifier produces a current pulse following each of the clock signal edges wherein the magnitude of the current pulse is a function of the magnitude of the analog signal and the magnitude represented by the adaption signal.

21. The method in accordance with claim 15 wherein step d comprises the substeps of:

d1. generating in response to the prediction signal and the adaption signal an analog signal having a magnitude that is a function of the magnitudes represented by the prediction signal and the adaption signal, and

d2. temporarily applying the analog signal as input to the amplifier following each of the clock signal edges, such that the amplifier produces a current pulse following each of the clock signal edges wherein the magnitude of the current pulse is a function of the magnitude of the analog signal.

22. The method in accordance with claim 15 wherein step d comprises the substeps of:

d1. responding to the prediction signal by charging a capacitor to a capacitor voltage that is a function of the magnitude represented by the prediction signal prior to each of the clock signal edges; and

d2. temporarily connecting the capacitor as input to the amplifier following each of the clock signal edges, such that the amplifier produces a current pulse following each of the clock signal edges wherein the magnitude of the current pulse

is a function of the magnitude of the capacitor voltage and the magnitude represented by the adaption signal.

23. The method in accordance with claim 15 wherein step d comprises the substeps of:

d1. responding to the prediction signal by producing an output signal of voltage that is a function of the magnitude represented by the prediction signal;

d2. responding to the adaption signal by adjusting a gain of an amplifier powered by the output signal produced at step d1; and

d3. temporarily applying a signal pulse as input to the amplifier following each of the clock signal edges, such that the amplifier produces a current pulse in response to each signal pulse, wherein the magnitude of the current pulse is a function of the voltage of the output signal's voltage and of the magnitude represented by the adaption signal.

24. The method in accordance with claim 15 wherein the magnitude represented by the adaption signal is adjusted by feedback to so as to minimize variations in the voltage appearing at the power input terminal,